

74LVQ157 Low Voltage Quad 2-Input Multiplexer

General Description

The LVQ157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non inverted) form. The LVQ157 can also be used as a function generator.

Features

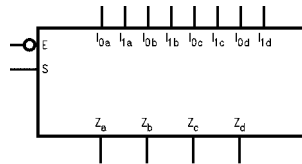
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω.

Ordering Code:

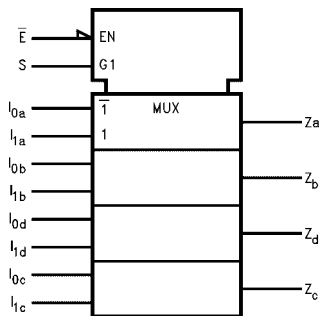
Order Number	Package Number	Package Description
74LVQ157SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVQ157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

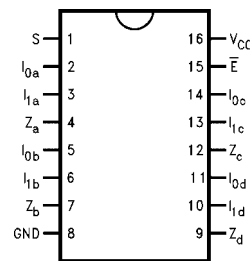
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
\bar{E}	Enable Input
S	Select Input
Z_a-Z_d	Outputs

Truth Table

Inputs				Outputs
\bar{E}	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Functional Description

The LVQ157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVQ157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

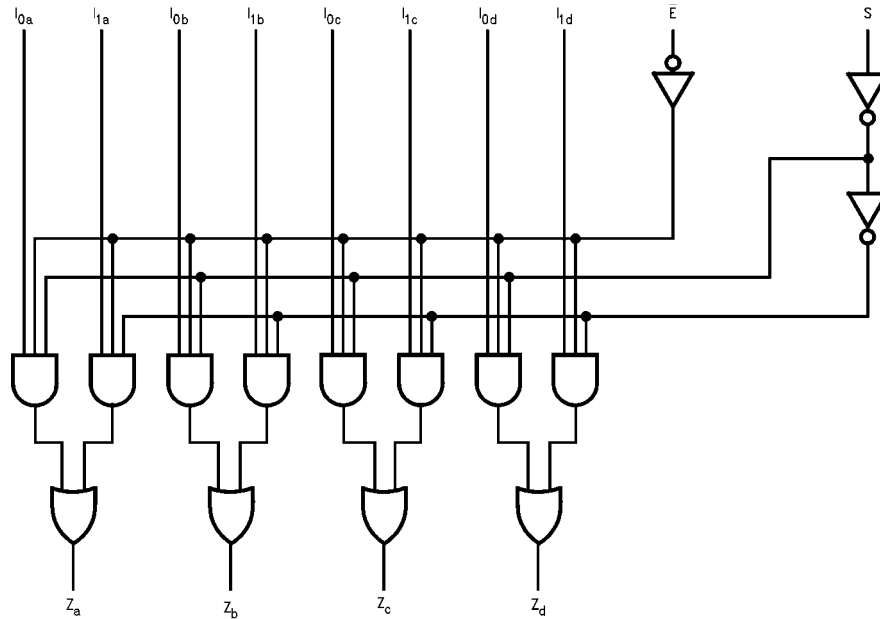
$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the LVQ157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVQ157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)			
Supply Voltage (V_{CC})		-0.5V to +7.0V	Supply Voltage (V_{CC})			2.0V to 3.6V
DC Input Diode Current (I_{IK})			Input Voltage (V_I)			0V to V_{CC}
$V_I = -0.5V$		-20 mA	Output Voltage (V_O)			0V to V_{CC}
$V_I = V_{CC} + 0.5V$		+20 mA	Operating Temperature (T_A)			-40°C to +85°C
DC Input Voltage (V_I)		-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)			
DC Output Diode Current (I_{OK})			V_{IN} from 0.8V to 2.0V			
$V_O = -0.5V$		-20 mA	V_{CC} @ 3.0V			125 mV/ns
$V_O = V_{CC} + 0.5V$		+20 mA				
DC Output Voltage (V_O)		-0.5V to $V_{CC} + 0.5V$				
DC Output Source						
or Sink Current (I_O)		± 50 mA				
DC V_{CC} or Ground Current						
(I_{CC} or I_{GND})		± 200 mA				
Storage Temperature (T_{STG})		-65°C to +150°C				
DC Latch-Up Source or						
Sink Current		± 100 mA				
DC Electrical Characteristics						
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$		Units	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	V	$I_{OUT} = -50 \mu A$
		3.0		2.58	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OH} = -12$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	V	$I_{OUT} = 50 \mu A$
		3.0		0.36	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic Output Current (Note 4)	3.6			mA	$V_{OLD} = 0.8V$ Max (Note 5)
I_{OHD}	Maximum Dynamic Output Current (Note 4)	3.6			mA	$V_{OHD} = 2.0V$ Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.7	0.8	V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	-0.4	-0.8	V	(Note 6)(Note 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Note 6)(Note 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Note 6)(Note 8)
<p>Note 3: All outputs loaded; thresholds on input associated with output under test.</p> <p>Note 4: Maximum test duration 2.0 ms, one output loaded at a time.</p> <p>Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for.</p> <p>Note 6: Worst case package.</p> <p>Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.</p> <p>Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1$ MHz.</p>						

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay S to Z _n	2.7	1.5	8.4	16.2	1.5	19.0	ns
		3.3 ± 0.3	1.5	7.0	11.5	1.5	13.0	
t _{PHL}	Propagation Delay S to Z _n	2.7	1.5	7.8	15.5	1.5	17.0	ns
		3.3 ± 0.3	1.5	6.5	11.0	1.5	12.0	
t _{PLH}	Propagation Delay E to Z _n	2.7	1.5	8.4	16.2	1.5	19.0	ns
		3.3 ± 0.3	1.5	7.0	11.5	1.5	13.0	
t _{PHL}	Propagation Delay E to Z _n	2.7	1.5	7.8	15.5	1.5	17.0	ns
		3.3 ± 0.3	1.5	6.5	11.0	1.5	12.0	
t _{PLH}	Propagation Delay I _n to Z _n	2.7	1.5	6.0	12.0	1.0	13.0	ns
		3.3 ± 0.3	1.5	5.0	8.5	1.0	9.0	
t _{PHL}	Propagation Delay I _n to Z _n	2.7	1.5	6.0	11.3	1.0	13.0	ns
		3.3 ± 0.3	1.5	5.0	8.0	1.0	9.0	
t _{OSHL}	Output to Output Skew (Note 9)	2.7		1.0	1.5		1.5	ns
t _{OSLH}	Data to Output	3.3 ± 0.3		1.0	1.5		1.5	

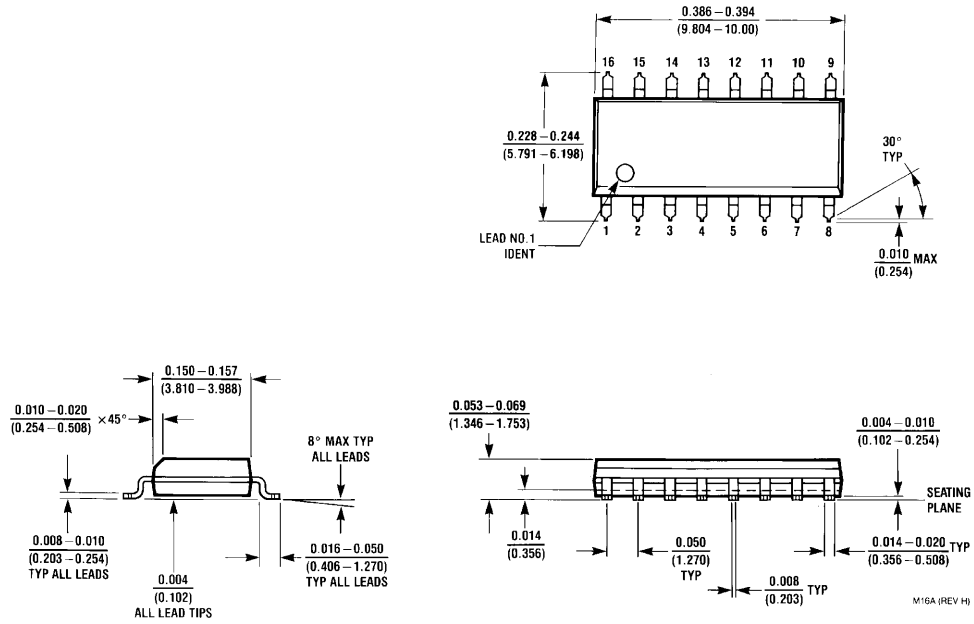
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _C = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	34.0	pF	V _{CC} = 3.3V

Note 10: C_{PD} is measured at 10 MHz.

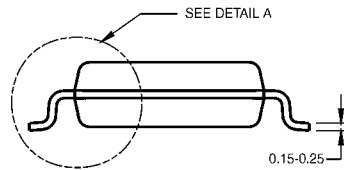
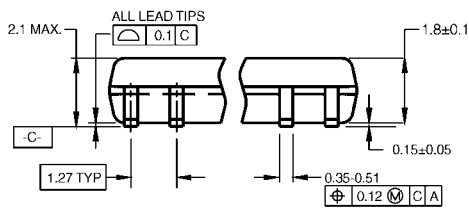
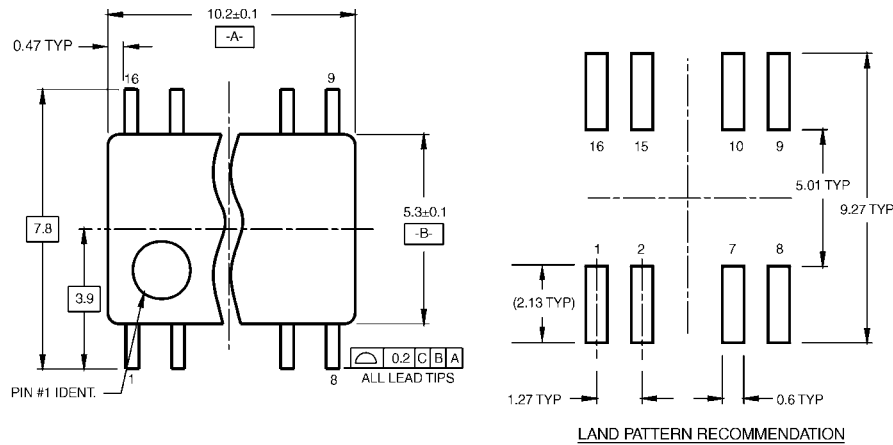
Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

M16A (REV H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

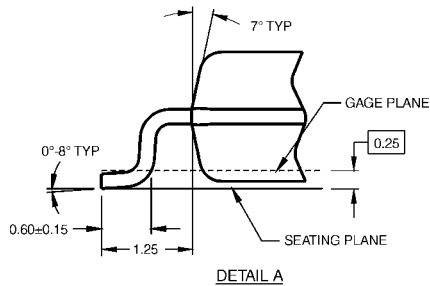


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

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